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<u>L5</u>	L3 and ((semiconductor or (integrated adj2 circuit\$2)) with memory with (cpu or processor) )	46	<u>L5</u>
<u>L4</u>	L3 and ((semiconductor or (integrated adj2 circuit\$2)) same memory same (cpu or processor) )	81	<u>L4</u>
<u>L3</u>	L2 or l1	608	<u>L3</u>
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**1 A 34 word×64 b 10 R/6 W write-through self timed dual-supply-voltage register file**

*Tzartzanis, N.; Walker, W.W.; Nguyen, H.; Inoue, A.;*  
Solid-State Circuits Conference, 2002. Digest of Technical Papers.  
ISSCC. 2002 IEEE International , Volume: 1 , 3-7 Feb. 2002  
Page(s): 416 -478 vol.1

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**1 A low power SRAM using auto-backgate-controlled MT-CMOS**

*Nii, K.; Makino, H.; Tujihashi, Y.; Morishima, C.; Hayakawa, Y.; Nunogami, H.; Arakawa, T.; Hamano, H.;*

Low Power Electronics and Design, 1998. Proceedings. 1998 International Symposium on , 10-12 Aug. 1998  
Page(s): 293 -298

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